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SEAT No. :

P1024

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[4457] - 223
S.E. (IT) (Semester - I)
DIGITAL ELECTRONICS AND LOGIC DESIGN
(2012 Course)

Time : 2 Hours] *[Max. Marks : 50*

Instructions to the candidates :

1) ***Answer Question 1 or 2, 3 or 4, 5 or 6 and 7 or 8.***
2) ***Neat diagrams must be drawn wherever necessary.***
3) ***Figures to the right indicate full marks.***
4) ***Assume suitable data, if necessary.***

Q1) a) Perform the following operations using 2's complement method. **[6]**

i) $-(48)_{10} - (23)_{10}$

ii) $-(48)_{10} (-23)_{10}$

b) Compare totem pole and open collector output configurations in TTL. **[6]**

OR

Q2) a) Draw and explain 2 inputs TTL NAND gate with Totem Pole Output. **[6]**

b) Design Full adder using suitable Decoder. **[6]**

Q3) a) What is Race around condition? How it can be avoided? Convert D Flip-Flop to T Flip-Flop. **[6]**

b) Explain with a neat diagram working of 3 bit bidirectional shift register. **[6]**

OR

Q4) a) Explain the difference between Combinational and Sequential Circuit. Design S-R Flip-Flop using J-K Flip-Flop. **[6]**

b) Design a sequence detector to detect the sequence ------- 110 ------- using J-K Flip-Flop. **[6]**

Q5) a) Explain difference between PAL & PLA. **[6]**

b) Design a 4 bit BCD to Excess-3 code converter using PLA. **[7]**

OR

Q6) a) Explain difference between FPGA & CPLD. **[6]**

b) Design the following function using PLA. **[7]**

$F_1 = \Sigma m (1, 2, 4, 6)$ $F_2 = \Sigma m (0, 1, 6, 7)$ $F_3 = \Sigma m (2, 6)$

P.T.O.

Q7) a) Explain entity and architecture in VHDL with syntax and example. **[6]**

b) Explain Process statement in behavior model of VHDL with respect to syntax, sensitivity list, declarative part and statement part. **[7]**

OR

Q8) a) Explain the difference between VHDL Modeling styles-Data Flow, Behavioral and Structural. **[6]**

b) Explain data objects in VHDL - signals, variables and Constants. **[7]**