Total No. of Questions—**8**] [Total No. of Printed Pages—**4**

Seat No.	

[4657]-582

S.E. (Information Technology)

(First Semester) EXAMINATION, 2014

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2012 PATTERN)

Time : Two Hours **Maximum Marks : 50**

N.B. **:—** (*i*) Answer Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**, Q. No. **7** *or* Q. No. **8**.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Assume suitable data if necessary.

1. (*a*) (*i*) Subtract $(27.50)_2$ from $(68.75)_2$ using 2's complement method. [4]

(*ii*) Explain the TTL characteristics-speed of operation and Fan-out. [2]

(*b*) Design Full adder using 4 : 1 multiplexer. [6]

P.T.O.

Or

2. (*a*) Convert the following numbers, show all the steps : [6]

(*i*) $(101101.10101)_2 = (\quad)_{10}$

(*ii*) $(247)_{10} = (\quad)_8$

(*iii*) $(0.BF85)_{16} = (\quad)_8$

(*b*) Compare TTL and CMOS logic family. Draw CMOS NOR gate. [6]

3. (*a*) Design JK flip-flop using SR flip-flop. [6]

(*b*) Design sequence detector to detect the sequence----1011---- using JK-flip-flop. [7]

Or

4. (*a*) Design and draw logic diagram of Mod-82 counter using IC7490. [6]

(*b*) Draw the ASM chart of washing machine with the following conditions : [7]

(*i*) Start the machine

(*ii*) Drain the previous existing water

(*iii*) Choose HOT or COLD water option

(*iv*) Pump in fresh water to fill washer tub

(*v*) Complete Washing cycle

(*vi*) Complete Rinsing cycle

(*vii*) Complete Drying cycle.

Assume the following inputs :

(1) H/C 1 = HOT, 0 = COLD

(2) Start 1 = Start, 0 = Stop

(3) Empty 1 = Washer tub completely empty 0 = Washer tub is full

(4) Time 1 = Time is over 0 = Time is not over.

5. (*a*) Design full subtractor using PLA. [6]

(*b*) Explain difference between PAL and PLA. [6]

Or

6. (*a*) Draw and explain the structural block diagram of FPGA. [6]

(*b*) Explain the difference between CPLDs and FPGAs. [6]

7. (*a*) What is VHDL ? Write features of VHDL. Explain the structure of VHDL module. [6]

(*b*) Explain the following three data objects—

variables, constants and signals

used in VHDL code with respect to need, location of declaration in VHDL module, syntax and example. [7]

Or

8. (*a*) Explain the difference between concurrent and sequential statements with example. [6]

(*b*) Write entity, architecture and package declaration for 3 bit synchronous up/down counter with asynchronous clear input. [7]